Materials Science Forum Vols. 457-460 (2004) pp. 905-908
online at http://www.scientific.net

Characterization of electrical properties in high-dose implanted and post-implantation-annealed 4H-SiC wafers using infrared reflectance spectroscopy

K.Narita[1], Y.Hijikata[1], H.Yaguchi[1], S.Yoshida[1,2], J.Senzaki[2], and S.Nakashima[2]

[1] Department of Electrical and Electronic Systems, Faculty of Engineering, Saitama University
255 Shimo-ohkubo, Sakura-ku, Saitama-shi, Saitama 338-8570, Japan

[2] Power Electronics Research Center, Nat. Inst. of Advanced Industrial Science and Technology
AIST Tsukuba Central2, 1-1-1 Umezono, Tsukuba-shi, Ibaraki 305-8568, Japan

Keywords: 4H-SiC, Ion implantation, Activation anneal, Infrared reflectance spectroscopy, Hall measurements, Carrier concentration, Mobility, Crystalline damage

Abstract. Infrared reflectance spectroscopy has been used to characterize the electrical properties and crystalline damage of high-dose implanted and post-implantation-annealed 4H-SiC. The carrier concentration, mobility and crystalline damage were independently derived from the analysis of the infrared reflectance spectra using the effective medium approximation and the modified dielectric function taking into account the TO and LO phonon damping factors independently. The carrier concentration and mobility in the recrystallized SiC derived from infrared reflectance spectra are in good agreement with those obtained from Hall effect measurements. The annealing temperature dependence of crystalline damage suggests that the impurities are almost activated by the annealing at a temperature as low as 1200°C for 30 min, though the crystallinity of the implanted layer is improved with increasing annealing temperature. In addition, it is revealed that the annealing at a temperature as high as 1700°C recovers the crystallinity of the implanted layer within 1 min. These results demonstrate that the infrared reflectance spectroscopy is a useful technique to characterize both the electrical properties and crystalline damage of implanted and post-implantation-annealed layers in SiC wafers simultaneously.

Introduction

Ion implantation is an indispensable process for selective area doping into crystalline silicon carbide (SiC). After the ion implantation, annealing at high temperatures is necessary for activating the dopants electrically as well as recovering the crystallinity of SiC damaged by ion implantation. Hall effect measurements, secondary ion mass spectroscopy (SIMS) and transmission electron microscopy (TEM) have widely been used to characterize the electrical properties, depth profile of the impurities and crystalline damage of implanted layers, respectively. These techniques are, however, inappropriate for device process monitoring tools because Hall effect measurement requires the formation of electric contacts, and SIMS and TEM observations result in the destruction of the samples.

Recently, it has been reported that the crystalline damage induced by ion implantation affects the infrared (IR) reflectance spectra around the reststrahlen region (~800-1000 cm^{-1}) [1,2], and the difference of carrier concentration between epitaxial layer and substrate induces the interference oscillation in the near IR region (1000-4500 cm^{-1}) [3]. In the present study, we have performed the infrared reflectance measurements in the spectral range between 600 and 8000 cm^{-1} for high-dose phosphorus ion implanted and post-implantation-annealed 4H-SiC wafers to characterize both the electrical properties and crystalline damage of the implanted layers without destruction.

Experimental Procedures

The samples used in this study were 4H-SiC (0001) substrates with p-type ~5 μm thick epitaxial layers (Cree Research Inc.). The multi-energy implantations of phosphorus ions at 500°C were carried out through the 10 nm thick oxide film in six steps (40-250 keV) in order to form a box-shaped profile with a thickness of 0.3 μm. The total implanted dose was $7x10^{15}$ cm^{-2} . After removing the oxide film by HF, the post implantation annealing was conducted in Ar atmosphere. To investigate the annealing temperature dependence of crystalline recovery and electrical properties in the implanted layers, the samples were annealed for 30 min at different temperatures of 1200 °C, 1300 °C, and 1400 °C. In addition, to apply the IR reflectance analysis to the short-period high-temperature annealing process [4], we also carried out the post-implantation annealing at 1700 °C for various periods between 0.5 and 10 min. Infrared reflectance measurements were carried out at room temperature on nearly normal incidence using a micro FT-IR spectrometer (light diameter was 0.1 mm). The spectral resolution and range were 4 cm^{-1} and 600-8000 cm^{-1}, respectively.

Results and Discussion

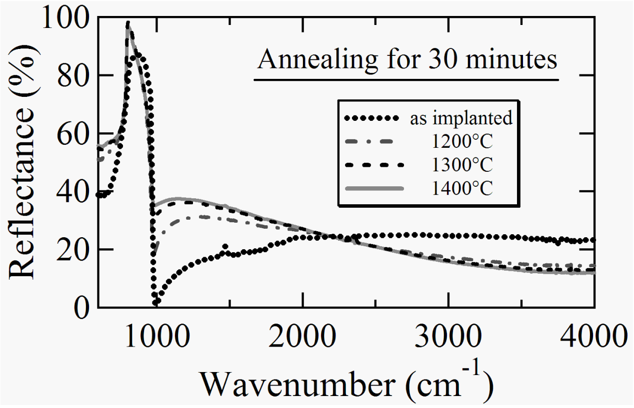

Fig. 1. The infrared reflectance spectra obtained from the 4H-SiC wafers high-dose implanted and post implantation anneald for 30 minutes.

Figure 1 shows the annealing temperature dependence of infrared reflectance spectrum. For as-implanted samples, the reflectivity maximum and the shape in the reststrahlen band decreases and becomes blunt, respectively, as compared to those of unimplanted samples. After the high temperature annealing, the reflectivity maximum in the reststrahlen band recovers to that of unimplanted samples. This results from the crystalline recovery in the implanted layer. In the spectral range above ~2000 cm^{-1}, the evident interference oscillation is observed. This indicates that the implanted dopants are electrically activated and that the refractive index of an implanted layer is changed by the increase in carrier concentration. We analyzed the measured spectra to evaluate the damage in the ion implantation layers assuming that the implanted layers are composed of two phases, recrystallized SiC phase and defective SiC phase. We have derived the effective dielectric constants e_{eff} of implanted layers using an effective medium approximation (EMA) [1], where the volume fractions of recrystallized and defective phases are given as 1-f and f, respectively. We assumed that the frequency dependence of both the dielectric constants of recrystallized and defective phases follows the modified dielectric function [5], which deal with the TO and LO phonon damping factors independently, as

$$e(w) = e_{\infty}\left(\frac{w_L^2 - w^2 - iG_L w}{w_T^2 - w^2 - iG_T w} - \frac{w_p^2}{w(w + ig_p)}\right) \quad . \tag{1}$$

The free carrier concentration N and mobility m can be derived using the relations of $w_p^2 = N \cdot e^2 / (m^* \cdot e_{\infty})$ and $m = e / (m^* \cdot g_p)$, respectively [6]. For the values of parameters such as w_T, w_L, e_{∞}, and m^* for crystalline 4H-SiC, we used those obtained from Raman scattering spectroscopy [7]. Referring to the result of TEM and SIMS studies, we employed the structural model that the implantation layer is composed of three layers: an undamaged surface layer, a carrier-concentration- plateau layer, and a graded-carrier-concentration layer (depicted in Fig. 2). Based on the cross sectional TEM images, we assumed that the volume fraction of the defective phase in a graded-carrier-concentration layer is the same as that in a carrier-concentration-plateau layer. For the graded-carrier-concentration layer, we used the multi-layer structure approximation assuming that the free carrier concentration decreases exponentially with depth and the mobility changes in inverse proportion to carrier concentration.

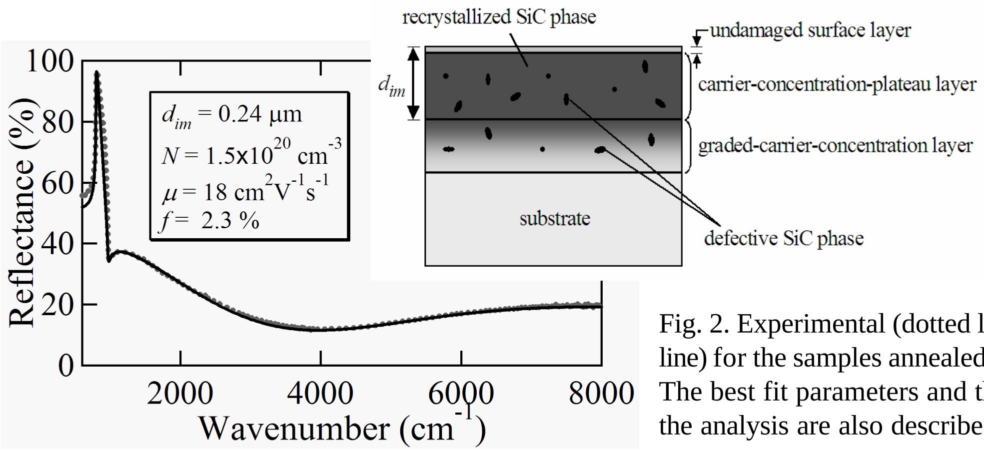

Fig. 2. Experimental (dotted line) and fitted spectra (solid line) for the samples annealed at 1400 °C for 30 minutes. The best fit parameters and the structual model used for the analysis are also described in the figure.

As an example of curve fitting analysis, the spectrum of the sample annealed at 1400°C for 30 min and the fitted curve are shown in Fig. 2. We obtained the good fit in a whole spectral region measured. The best-fit parameters derived are also described in the figure.

The thickness of an undamaged surface layer, a carrier-concentration-plateau layer, and a grated-carrier-concentration layer obtained are around 0.02, 0.22, and 0.08 μm, respectively. Figure 3 (a) shows the annealing temperature dependence of the volume fraction of the defective phase. By post implantation annealing, the volume fraction of defective SiC is decreased drastically from 92 % (as implanted) to 2.9 % (1200°C annealed), and is decreased a little with increasing annealing temperature up to 1400 °C. Figure 3 (b) shows the annealing temperature dependence of the carrier concentration (open circle) and the mobility (open triangle) in the recrystallized phase. For comparison, the electrical properties derived from Hall effect measurements [4] are also plotted in the figure. We can see a good agreement between the electrical properties derived from the infrared reflectance spectroscopy and those from Hall effect measurement. The free carrier concentrations are almost constant in the temperature range studied, as well as that of the volume fraction of defective phase. In contrast, the carrier mobility becomes larger with increasing annealing temperature. These results show that the post implantation annealing at a temperature as low as 1200 °C decreases the volume fraction of defective SiC drastically, and put the impurities onto substitutional lattice sites. However, the crystalline recovery of the recrystallized phase is insufficient. In other words, the annealing temperature higher than 1400 °C is necessary for

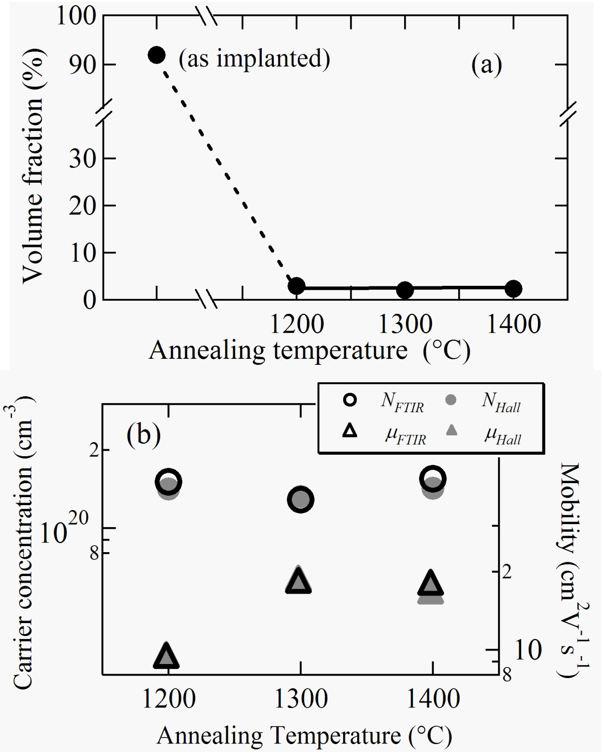

Fig. 3. The annealing temperature dependence of (a) volume fraction of defective SiC phase, and (b) free carrier concentration and mobility in recrystallized SiC phase. The values determined from Hall effect measurement also plotted in (b) for comparison.

improving the mobilities, as well as for activating the impurities.

Recently, it has been reported that the short period and high temperature annealing is used in SiC device process [4]. Figure 4 shows the infrared reflectance spectra for the samples annealed at 1700 °C for various annealing times. The spectrum for the sample annealed at 1700 °C for 0.5 min is almost the same as that for the sample annealed at 1400 °C for 30 min. In the case of 1700 °C annealing, the spectra change little with annealing time from 0.5 to 10 min except for the oscillation periods. Since the oscillation periods are concerned with the thickness of the implanted layer, these changes suggest that the thickness of the implanted layers is reduced by sublimation during long period annealing. The volume fraction of defective SiC is decreased drastically down to 2.9 % by 0.5 min annealing and is almost constant up to 10min. The derived annealing time dependence of free carrier concentration and mobility also shows that the recovering of the crystallinity and the electrical activation are sufficient by the annealing even for 0.5 min. These results indicate that the high temperature annealing as high as 1700 °C puts the impurities onto substitutional lattice sites and recovers the crystallinity of the implanted layers within 1 min.

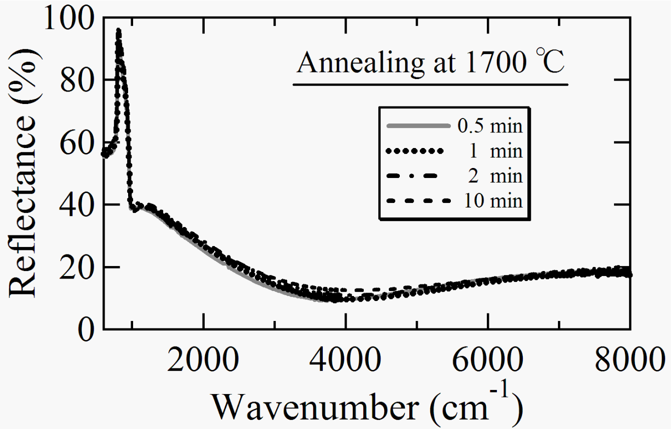

Fig. 4. The infrared reflectance spectra obtained from the samples annealed at 1700 °C for various periods.

Conclusions

We have performed the infrared reflectance spectroscopy measurements to characterize both the electrical properties and crystalline damage in high-dose phosphorous implanted and post implantation annealed layers. From the analysis of the measured spectra, we can see the good agreement in electrical properties such as free carrier concentration and mobility with those obtained from Hall measurements. It is revealed that the impurities are activated by annealing at a temperature as low as 1200 °C for 30 min, though the sufficient recovery of the crystallinity needs higher annealing temperatures than 1200 °C. It is also found that the annealing at 1700 °C activates the impurities and recovers the crystallinity of implanted layer within 1 min.

The results of the present work suggest that the infrared reflectance spectroscopy is a useful technique as a device-process monitoring tool in order to characterize both the electrical properties and crystalline damage of the implanted layers in SiC wafers simultaneously.

References

[1] W. Chang, Z. C. Feng, J. Lin, R. Liu, A. T. S. Wee, L. Tone, and J. H. Zhao: Surf. Interface Anal., Vol. 33,500 (2002).

[2] J. Camassel, H. Y. Wang, J. Pernot, P. Godignon, N. Mestres, and J. Pascual: Mater. Sci. Forum, Vol. 389-393, 859 (2002).

[3] M. F. Macmillan, A. Henry, and E. Janzen: J. Electron. Mater., Vol. 27, 300 (1998).

[4] J. Senzaki, K.Fukuda, and K. Arai: J. Appl. Phys., Vol. 94, 2942 (2003).

[5] J. Camassel, J. Pernot, H. Y. Wang, and H. Peyre: phys. stat. sol. (a), Vol. 195, 38 (2003).

[6] H. Yaguchi, K. Narita, Y. Hijikata, S. Yoshida, S. Nakashima and N. Oyanagi: Mater. Sci. Forum, Vol. 389-393, 621 (2002)

[7] H. Harima, S. Nakashima, and T. Uemura: J. Appl. Phys., Vol. 78, 1996 (1995).