Effect of Ar post-oxidation annealing on oxide–4H-SiC interfaces studied by capacitance to voltage measurements and photoemission spectroscopy

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The effect of post-oxidation annealing in Ar atmosphere (Ar POA) on 4H-SiC–oxide interfaces has been studied by capacitance to gate-bias voltage (C-V) measurements and photoemission spectroscopy (PES). It was found from the C-V measurements that the shift of the C-V curve disappears when the Ar POA temperature is higher than 600 °C. On the other hand, angle-resolved x-ray photoelectron spectroscopy measurements revealed that the thickness of the intermediate layers containing Si¹⁺ oxidation states observed at the interfaces decreases abruptly when the Ar POA temperature exceeds 500 °C. In ultraviolet photoelectron spectra, O2*p* peaks were changed by Ar POA at temperatures higher than 600 °C, which is the temperature where the shift of the C-Vcurve disappears in C-V measurements. This shows that the change in O2*p* bonding by Ar POA is the origin of the shift observed in C-V characteristics. A model of structural changes in the interfaces by Ar POA has been proposed based on the results of PES measurements and those of C-V measurements. © 2005 American Vacuum Society. [DOI: 10.1116/1.1865153]

I. INTRODUCTION

The physical properties of silicon carbide (SiC), such as a wide bandgap and a high-breakdown electric field, are attractive for high-power and high-frequency electronic devices whose specifications are difficult to obtain using Si or GaAs. In addition, SiC can be thermally oxidized to form insulating SiO₂ layers, which are known to have superior dielectric properties for metal-oxide-semiconductor (MOS) applications, similar to Si.¹ However, SiC MOS field-effecttransistors (FETs) have some problems to be solved before practical use, such as their higher on-resistances than those predicted from bulk properties of SiC. This poor electrical characteristic is considered to be due to the low channel mobility in inversion layers of SiC MOSFETs,² and the low channel mobility results from the high interface trap density and large oxide traps.^{3,4} It has been reported that some postoxidation processes, such as NO annealing⁵ and re-oxidation,^{6,7} improve electrical characteristics of SiC MOS capacitors and/or MOSFETs. A post-oxidation annealing in Ar atmosphere (Ar POA) is well-known as a thermal annealing by an inert gas and is effective in reducing flatband voltage.⁴ In our recent work,⁸ capacitance to gate-bias voltage (C-V) measurements for the sample before Ar annealing showed that the C-V curve shifts toward the higher gate-bias voltage side when increasing the sweep range of the gate-bias voltage. It was also found that this shift disappears by Ar POA at temperatures higher than 600 °C.

A number of photoemission spectroscopic (PES) studies have been carried out to make clear the structure of oxide– SiC interfaces.^{9–16} Although these reports provide some information about the structure of the interface, this information does not extend to the mechanism of the electrical improvement due to the post-oxidation processes, even the thermal annealing.

In this report, we have studied the changes in charges trapped near the interface and in the structure of SiC-oxide interfaces due to Ar POA at various temperatures by using C-V measurements and angle-resolved x-ray and ultraviolet photoelectron spectroscopy (AR-XPS and UPS), respectively. We also discuss the structural changes of SiC-oxide interfaces by Ar POA and the reason for the improvement of electrical characteristics.

II. EXPERIMENTS

Epitaxial wafers of 4H-SiC with 8° off-oriented (0001) Si-face, *n*-type, $N_d - N_a = 6 \times 10^{15}$ cm⁻³ were used. After a standard RCA cleaning, eight SiC epitaxial films were oxidized up to 50 nm in oxide thickness in high-purity dry O₂ flow at 1200 °C. The dew point of the O₂ flow used was below -100 °C. After the oxidation, two films were cooled to room temperature quite quickly [denoted "quenched" (a)]. The other samples were followed by annealing in Ar atmo-

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sphere for 3 h at various temperatures: (b) 500 °C, (c) 600 °C, and (d) 950 °C. We deposited Au 0.5 mm in diameter as gate electrodes and Al as ohmic electrodes on the surfaces and the backside surfaces of the samples, respectively, for *C*–*V* measurements. High-frequency *C*–*V* measurements were performed with a driving frequency of 1 MHz under dark condition at room temperature. The samples for PES measurements were etched off by buffered HF solution down to the thickness in the order of the photoelectron escape depth ($\lambda_e \sim 2.3$ nm for XPS and ~1.5 nm for UPS), to observe the bonding states at the interfaces. From the spectroscopic ellipsometry measurements, the oxide thickness (d_{ox}) of samples (a)–(d) were found to be around 2 nm. After all the PES measurements were done, samples (a) and (d) were further etched down to 1 nm.

In the present work, the samples used for C-V and PES measurements were fabricated at the same time because the electrical characteristics of the oxide–SiC structure are very sensitive to the oxidation conditions.⁸ Also in a previous paper, we showed that the structures of the interface layers of thick oxide films are different from those of ultra-thin oxide films.¹⁷ Accordingly, we did not use ultra-thin oxide films, but rather, etched back ones for PES measurements to compare with the results of electrical measurements of MOS structures using thick oxide films.

AR-XPS measurements were done with the nonmonochromatized Mg-K α line (1253.6 eV) as a light source and a semispherical analyzer as an electron spectrometer. After AR-XPS measurements were carried out, Au thin films were deposited on a part of the sample surfaces for the energy references. UPS measurements were performed with the He II line (40.8 eV) as a light source.

III. RESULTS AND DISCUSSION

A. Capacitance to voltage measurements

Because SiC is a wide-bandgap semiconductor, carrier trap states are likely to appear at deep levels. In this case, the carrier charging and releasing time of such states is very long. Therefore, the "true" C-V characteristics cannot be obtained unless we make the sweep gate-voltage extremely slow. In addition, an insulation breakdown or leakage current may occur due to the over-voltage applied in the case that such deep-level states are not filled with carriers.¹⁸ The extension of the range of gate voltage from the narrow range is useful for avoiding this situation. Accordingly, we first swept the gate-voltage from +2 to -2 V, i.e., [+2 V, -2 V]. Next, the sweep range was extended to [+4 V, -2 V], and then, $[+6 \text{ V}, -2 \text{ V}] \cdots [+22 \text{ V}, -2 \text{ V}]$ (whose detail have been described as "cycle C-V measurements" in Ref. 8). The shift in C-V curve due to the interface trap charge, as we will show later, was not observed unless we sweep the gatevoltage from a positive to a negative side, i.e., from the accumulation side to the inversion side. We consider that once the carrier are kept away from the interface states by a negative gate-voltage, they cannot follow the sweeping speed of the gate-voltage. Hence, a part of the information about the



FIG. 1. Cycle C-V characteristics of 4H-SiC MOS structures for sample (a).

interface states disappear in the C-V characteristics obtained. For this reason, we swept from a positive to a negative gatevoltage in our C-V measurements. We determined 2 V as the beginning gate-voltage of the first sweep because this voltage is high enough to cancel the shift in C-V curve due to other than the interface trap charge. Also it is low enough to avoid the influence of a transient state in the capacitance output by filling the interface state density near the conduction-band edge, which is known to be extremely high for the oxide–SiC systems.¹⁹

Figure 1 shows the results of the cycle C-V measurements for the quenched sample (a). The number in the figure indicates the trial number of the sweep of gate-voltage. We could not measure the capacitance over +22 V in gate-voltage because an insulation breakdown of the oxide film occurred. However, the capacitance at +22 V is almost the same as the insulator capacitance estimated from the oxide thickness of the sample, denoted as C_{ox} in the figure. Therefore, the C-Vcurve obtained contains the information because the accumulation layer have already formed at this gate-voltage. The notations $(C_{std} \text{ and } C_{fb})$ in the figure show the maximum capacitance obtained for the first sweep of gate-voltage and the capacitance corresponding to the flat-band condition, respectively. It is found from the figure that the capacitance does not exceed the $C_{\rm std}$ until the eighth sweep. This indicates that many acceptorlike interface states exist around the energy level corresponding to $C_{\rm std}$. As we mentioned before, the measured capacitance in the 11th sweep is almost the same as the C_{ox} level. This means that no more positive shift in C-V curve may occur after the 11th sweep. The broken line in the figure shows the 11th C-V curve plotting on the position of the first sweep. We can see that a part of this broken line agrees with the first trial curve. This also indicates that the amount of negative charges arising from the interface states is proportional to the maximum gate-voltage corresponding to $C_{\rm std}$. Therefore, this displacement of the gate-voltage is a useful parameter to estimate the electrical property of the samples. Here, the range of gate voltage between the first applied voltage and the maximum voltage corresponding to $C_{\rm std}$ is defined as the cycle V_g shift $(\Delta V_g^{\text{cycle}})$. The values of $\Delta V_g^{\text{cycle}}$ and flat-band voltage (V_{fb}) for sample (a) were +10.8 and 16.5 V, respectively. After the 11th sweep was finished, we carried out the measurement



FIG. 2. Normalized cycle V_g shift $\Delta V_g^{\text{cycle}}$, net numbers of interface-trapped charges per unit area N_{it} , thickness of the intermediate layer d_1 , normalized O2*p* peak intensity $I(O_{\alpha})$ and $I(O_{\beta})$, energy gaps of interface layer E_g and valence-band offsets between them ΔE_v , as a function of POA temperature.

from the beginning of the sweep range again. The cycle V_g shift was not observed at all at that time. However, the cycle V_g shift reappeared after leaving the sample under opencircuit for 24 h. We also performed the cycle C–V measurements for *p*-type 4H-SiC MOS capacitors. The cycle V_g shift in the negative voltage direction was observed. Further, the reappearance of the shift after 24 hours under open-circuit was seen similarly in the case of *n*-type. Therefore, the origin of the cycle V_g shift in *p*-type may possibly be the same as that in *n*-type; in this case, it is bipolar defects.

Figure 2 shows $\Delta V_g^{\text{cycle}}$ and net numbers of interfacetrapped charges per unit area (N_{ii}) as a function of POA temperature. The values of N_{ii} s were obtained by the photo C-V measurements, whose experimental details are described in Ref. 8. We can see that $\Delta V_g^{\text{cycle}}$ decreases abruptly at 600 °C; in addition, the value at 500 °C scarcely changes from that of quenched samples. Conversely, N_{ii} increases gradually with increasing POA temperature, i.e., the value of N_{ii} at 500 °C differs from that of quenched samples. It is noted that the temperature dependence of $\Delta V_g^{\text{cycle}}$ is different from that of N_{ii} , especially at 500 °C.



FIG. 3. XPS spectrum of Si2p region from sample (a) at $\theta_e = 45^\circ$.



FIG. 4. Intensity ratios of the components as a function of θ_e for sample (a): Solid lines denoted as fitting curves calculated by the procedure in Ref. 14.

B. Angle-resolved XPS measurements

The circles in Fig. 3 show XPS spectrum of the Si2p region from the quenched sample (a) when an intake angle of photoelectron (θ_e) , which is regarded as an angle from the sample surface, equals 45°. The measured spectrum was decomposed into the component peaks with Gaussian including Lorentzian.¹⁴ The component peaks and the sum are shown by solid lines in the figure. Only an extra peak corresponding to the Si¹⁺ oxidation state is clearly seen, whereas, no other peaks such as Si²⁺ and Si³⁺ are seen.

The spectrum of the C1*s* region shows no peak corresponding to a C–O bond in all the samples. This result supports previous reports.^{12,14} Although some papers^{9–11,13,15,16} have reported that Si oxycarbide exists at the oxide–SiC interfaces, the extra peak appears to be a ghost peak due to the Lorentzian contribution.

The intensity ratios, Si⁴⁺-Si¹⁺, Si⁴⁺-Si⁰⁺, and Si¹⁺-Si⁰⁺, as a function of θ_e for the quenched sample (a) are shown in Fig. 4. The structure of oxide film on SiC can be estimated roughly from angle-resolved data by use of the two layers attenuation model.¹⁴ In this model, an oxide film is assumed to be composed of two layers, an intermediate oxidation layer containing Si¹⁺ state and a SiO₂ layer, as shown in the inset of Fig. 4, where d_1 and d_4 are the thickness of these layers, respectively. The photoelectron escape depth for the intermediate layer is assumed to be the same as that for SiO₂ (2.3 nm).¹⁵ The values of d_1 and d_4 for sample (a) were calculated as 0.30 and 1.75 nm, respectively. The same analyses were done for samples (b)-(d), as well. The results for d_1 are also shown in Fig. 2. We found that d_1 decreases slightly with increasing POA temperature. Also the temperature dependence of d_1 agrees with that of N_{it} , rather than that of $\Delta V_{\rho}^{\text{cycle}}$, because d_1 changes at 500 °C.

C. UPS measurements

Figure 5 shows UPS spectra of samples (a)–(d) at $\theta_e = 90^\circ$. The horizontal axis in the figure indicates the relative



FIG. 5. UPS spectra of ultra-thin oxide films on 4H-SiC at various POA temperatures at θ_e =90°.

energy from the SiC valence-band maximum (VBM). Here, the peaks around 5.5 eV and that around 9.8 eV in Fig. 5 are denoted as O_{α} and O_{β} , respectively. It has been reported in the case of an ultra-thin oxide film on Si that the twin peak observed at the energy region greater than 4.4 eV is assigned to O2p theoretically²⁰ and experimentally.²¹ In these reports, the peak observed at 7.0 eV and that at 10.5 eV below the Si VBM can be attributed to O2p nonbonding or π bonding at the top-most Si layer and to Si-O-Si bridge bonds between top-most and second-top-most Si layers, respectively. The former and the latter peaks are denoted as O_{π} and O_{i} , respectively. The relative energies of O_{π} and O_i correspond to 5.6 and 9.1 eV, respectively, below the SiC VBM if we assume the energy differences between vacuum level and the Si VBM and between that and SiC VBM are ~ 5.4 and \sim 6.8 eV, respectively.²¹ Taking into account that the energy position of the O_{α} peak is very close to that of O_{π} , and in addition, the surface reconstruction containing π bonding is unlikely to occur at the oxide–SiC interface, the O_{α} peak probably originates from O2p nonbonding. Because the energy of the O_{β} peak is close to that of O_i , and the O_{β} peak is the first peak immediately following the O_{α} peak, O_{β} can be



FIG. 6. UPS spectra of oxide films of 2 nm in thickness on 4H-SiC without POA and with 950 °C POA at various photoelectron in-take angles θ_c ; (i) θ_e =45°, (ii) θ_e =60°, (iii) θ_e =90°, (iv) θ_e =90° in case that d_{ox} =1 nm.



FIG. 7. A schematic energy-band diagram.

assigned to Si–O–Si bridge bonds. Figure 5 shows that the shape of the O2*p* twin peak changes remarkably by Ar POA. Also the temperature at which the shape of O2*p* changes, i.e., 600 °C, agrees well with the temperature at which the *cycle* V_g shift disappears, as mentioned before. Figure 6 shows the UPS spectra of samples (a) and (d) of 2 nm in oxide thickness at various values of θ_e and that of 1 nm in oxide thickness at θ_e =90°. The difference in the O2*p* twin peak between these samples becomes larger with increasing θ_e . By comparing (iii) with (iv), the change by Ar POA for 1 nm in oxide thickness is much larger than that for 2 nm. These results suggest that the change of O2*p* bonding structure by Ar POA occurs around the interface.

The changes of O2p twin peak by Ar POA are seen as the peak energy shift and the changes in peak intensity. The peak energy shift of O2p twin peaks by Ar POA observed in UPS measurements can be explained by the chemical shift arising from a stress at the interface layer¹² or the charge up around the interface. However, it has not been known which of these explanations are the reason for the shift. On the other hand, the change in the intensity of the O2p twin peak by Ar POA suggests that the amounts of both O2p nonbondings and Si–O–Si bridge bonds were reduced at the interface. The peak intensities of O_{α} and O_{β} normalized by those for sample (a), denoted as $I(O_{\beta})$ and $I(O_{\alpha})$, for samples (a)–(d) are also shown in Fig. 2. It is found that both of these temperature dependences agree well with that of the *cycle* V_g shift.

D. Analysis of oxide-SiC band lineup

The energy gap of the whole oxide layers and the valenceband offset between SiC and oxide layers, denoted as E_g and ΔE_v , can be obtained from the analysis of the O1s energyloss spectrum and that of the UPS spectra near the valenceband maximum, respectively.²² Figure 7 shows a schematic energy-band diagram. Figure 8 shows the schemiatic view of the procedure for obtaining E_g and ΔE_v , in the case of the quenched sample (a), for example. The value of E_g is obtained from the energy difference between the O1s peak energy and the kink point given by two solid lines, extracted



FIG. 8. Spectrum analysis for energy gap of whole oxide layer (i) and bandoffset between the valence-band maximum of SiC and that of interface oxide layer (ii): In case of sample (a).

from the background and the straight onset in the energy loss edge (shown in the upper figure in Fig. 8). The valence-band edge of the oxide layer is obtained by the subtraction of the spectrum for bare SiC from the measured spectrum normalized by the intensity around the SiC valence-band edge (~0-3 eV). As seen in Fig. 8(ii), it is obvious that the O2p region contributes to the valence-band edge of the oxide layers. Consequently, the value of ΔE_v corresponds to the energy difference between the valence-band edge of SiC and the lower-side edge of the O2p peak. All the values obtained are shown in Fig. 2. Although the values of band edges obtained include the error of ± 0.1 eV, the figure suggests that both of E_g and ΔE_v increase at the POA temperatures higher than 600 °C. The temperature dependence of these values agrees well with that of the *cycle* V_g shift.

As shown in Fig. 7, the fact that the value of E_g of the quenched sample is estimated apparently to be smaller than that of a stoichiometric SiO₂ and that of the Ar annealed sample is interpreted as the density of states due to the interface states near the band edge connects with the band. Therefore, the apparent increase of E_g by Ar POA means the reduction of interface states. We think that the reason for the increase of ΔE_v is the same as that for E_g because there is a good correlation between the temperature dependence of E_{g} and that of ΔE_v , as shown in Fig. 2. The large ΔE_v should result in the high interface state density near the conductionband edge because the density at this energy region usually increases with elevating the energy level. The high interface state density was observed actually as the large cycle V_{ρ} shift by the C-V measurements for the quenched sample. Therefore, this interpretation can explain the results from both the C-V and PES measurements.

IV. DISCUSSION OF RELATION BETWEEN ELECTRICAL CHARACTERISTICS AND INTERFACE STRUCTURES

Based on the results of PES measurements, consider the atomic arrangement of oxide-SiC interfaces and the structural change of the interfaces by Ar POA. We found from the AR-XPS measurements that only Si¹⁺ oxidation states exist at the interfaces and that their number decreases by Ar POA. From the results of UPS measurements, O2p nonbonding and Si-O-Si bridge bonding exist at the interface and their numbers also decrease by Ar POA. A Si¹⁺ oxidation state is considered to be attributable to C-Si*-O bonds, where the asterisk denotes the atoms in a Si topmost layer of SiC bulk layer, because no photoemission peak corresponding to a C-O bond is seen from the C1s region. On the other hand, the O2p photoemission peak originating from stoichiometric SiO₂, denoted as O_{σ} in Refs. 20 and 21, arises at 12.5 eV (the result is not shown here). Therefore, the binding energies of O_{α} and O_{β} are thought to be the smallest and second smallest, respectively, of those of the three. Together with the information from the core-level study, O2p nonbonding and Si-O-Si bridge bonding is thought to be attributed to an oxygen connecting with two Si*s and Si*-O-Si** bonds, respectively, where two asterisks denote the atoms in the oxide layer. Also, because these bonds and the thickness of the Si¹⁺ oxidation-state layer decrease by Ar POA, we may consider that this interfacial incomplete oxidation state such as Si*-O-Si* and Si*-O-Si** can be annealed out, and then the formation of Si**-O-Si** bonding occurs. However, the temperature dependence of the cycle V_g shift does not correspond to that of the thickness of Si¹⁺ oxidation state. Rather, the temperature dependence of the thickness of Si¹⁺ corresponds to that of N_{it} , especially at 500 °C in the POA temperature. We consider that the origin of N_{it} can be restricted not to one defect, but complexly to other various ones, although the origin of the cycle V_g shift is attributable to only the incomplete oxidation states.

V. SUMMARY

We have studied the effects of Ar POA on SiC-oxide interfaces by cycle C-V and AR-XPS/UPS measurements. We found from the cycle C-V and ultraviolet photoelectron spectroscopy (UPS) measurements that the cycle V_g shift disappears at 600 °C, and the O2p bonding of the interface changes drastically above this temperature. From the results of AR-XPS, only Si¹⁺ oxidation states exist, whereas C-O bonds do not exist at the interfaces. In addition, Si1+ states decrease with increasing POA temperature, and the temperature dependence corresponds to that of N_{it} . The temperature dependence of E_g and ΔE_v correspond to that of cycle V_g shift. Based on these results, the atomic structure of oxide-SiC interfaces and the effect of annealing on them were discussed. The incomplete oxidation bondings such as O_{α} and O_{β} states are suggested to be relevant to the negative charge bringing about the cycle V_g shift. Annealing of these bonds gives rise to a replacement to the stoichiometric SiO₂, resulting in a restraint of the negative charges.

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