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MOS capacitors obtained by wet oxidation of n-type 4H–SiC pre-implanted with nitrogen

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Abstract

The manufacture process and the electrical characterization of MOS devices fabricated by wet oxidation of N^+ implanted n-type 4H–SiC are here presented. Different implantation fluence and energy values were used with the aims to study the effect of the N concentration both at the SiO_2/SiC interface and within the SiO_2 film. High doses, able to amorphise a surface SiC layer to take advantage of the faster oxidation rate of amorphous with respect to crystalline SiC, were also evaluated. The electrical quality of the SiO_2/SiC system was characterized by capacitance–voltage measurements of MOS capacitors. The analyses of the collected data show that only the implanted N which is located at the oxide–SiC interfaces is effective to reduce the interface states density. On the contrary, the interface states density remains high (the same of an un-implanted reference sample) when the implanted N is completely embedded in the region consumed by the oxidation. Furthermore, none generation of fixed positive charges in the oxide was found as a consequence of the different N concentrations enclosed in the oxide films. These results were independent of the amorphisation of the implanted layer by the N^+ ions. Our results demonstrate that by using a suitable N ion implantation and an appropriate wet oxidation treatment, it is possible to obtain a reduced thermal budget process able to decrease the interface state density near the conduction band edge. The proposed approach should be interesting for the development of the MOSFET technology on SiC.
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Keywords: MOS capacitors; Nitrogen implantation; Interface states

1. Introduction

Crystalline SiC is the only wide band gap semiconductor with SiO_2 as native oxide. In addition, SiC has physical properties, such as high-breakdown electric field and high thermal conductivity, that make this material attractive for high-speed switching and low power-loss electronic devices. The electrical properties of SiO_2/SiC structure have been widely investigated [1] and the status of the art is that these properties need to be improved for MOSFET device applications. Once this will be achieved, SiC will be in an advantageous position for MOS-based power device applications in comparison to other wide band gap semiconductors. At the present among the electrical characteristics of SiC MOSFETs that are poorer than those predicted from SiC properties is the on-resistance. This device parameter is strongly degraded by the high SiO_2/SiC interface state density (D_{it}), especially from the states near the conduction band edge [2]. The detrimental effects of these interface traps are the reduction of the channel electron mobility and the increase of the Fowler–Nordheim tunneling current responsible of the dielectric degradation [3]. Another negative feature of MOSFET technology is the low oxidation rate of crystalline SiC which requires a high thermal budged for the growth of the gate oxide [1].

Many efforts have been devoted to reduce the interface state density at the SiO_2/SiC interface. Some articles reported that the D_{it} density reduces when wet ambient is

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used during the oxidation and/or in the post-oxidation annealing [4,5]. Also a thermal nitridation of oxide–SiC interfaces obtained by annealing of pre-grown oxide or direct oxide growth in NO or N_2O environment [6–9] has proved to reduce the D_{it} value. Finally, few investigations report about the use of a Nitrogen ion implantation process before the thermal dry-oxidation of SiC [10–12]. With respect to dry-oxidation of crystalline SiC, a pre-oxidation treatment by N implantation produces a strong reduction of D_{it} near the conduction band edge [10,11] associated to an increase of the interface traps near the valence band edge [12]. Drawback of such N implantation process is the increase of fixed positive charges in the oxide. The integral of these charges grows up proportionally with implanted dose, giving rise to an unwanted shift of the flat-band voltage (V_{fb}) [10,12]. On the base of this scenario, a further reduction of the interface states should be expected by joining N^+ implantation and wet oxidation in the manufacture process of a MOS structure. Moreover, if the N implantation process amorphised a SiC surface layer, the advantage of an enhanced oxidation rate like that shown in Ref. [13–15] might be exploited.

In this work, with the purpose to minimize the SiO_2/SiC interface state density, we fabricated MOS capacitors by wet oxidation of n-type 4H–SiC pre-implanted by nitrogen. We investigated a wide range of implantation doses, including a high dose able to amorphise a surface SiC layer and so to increase the oxidation rate. The oxide and the SiO_2/SiC interface characteristics have been evaluated by capacitance to voltage (C–V) measurements.

2. Experiments

An n-type 4H–SiC homoepitaxial wafer (8° off-axis, epilayer thickness = 6 μm, epilayer doping $N_d - N_a = 1 \times 10^{16}$ cm^{-3}) was employed for this study. The wafer was cut in quarters in order to obtain four samples (#1–#4). A 0.6 μm thick field oxide was deposited by CVD technique and patterned to open circular gate geometry of 750 μm in diameter. These samples were successively implanted at room temperature by N ions of different energy and dose values. Sample #2 was implanted at 10 keV with a dose of 1.5×10^{13} cm^{-2}, sample #3 at 2.5 keV with dose 1.0×10^{15} cm^{-2}, while sample #4 was double implanted at 2.5 and 5 keV with the same dose of 5.0×10^{14} cm^{-2} for each energy. An un-implanted sample, labeled #1, was also prepared for comparison. Table 1 summarizes these implantation parameters.

The as-implanted N distribution was computed by simulations and measured by secondary ion mass spectrometry (SIMS). The simulations are based on SRIM2003 code [16]. SIMS nitrogen profiles have been performed using a CAMECA Sc-Ultra mass spectrometer using Ce^+ as primary beam with impact energy of 500 eV. The sensitivity of the measurement for N profiles is 5×10^{18} cm^{-3}. Simulated and measured N profiles are shown in Fig. 1a and b, respectively. Due to the sensitivity limit of the SIMS measurements an accurate evaluation of the N profile in the sample implanted at the lowest dose (sample #2) was not possible.

Taking into account the above N distributions, the consumption of ~27 nm of SiC during the oxidation would

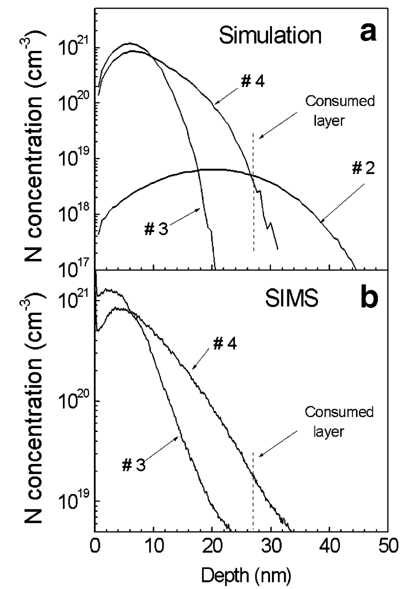

Fig. 1. As implanted N profiles in SiC computed by simulations for samples #2, #3 and #4 (a) and measured by SIMS for samples #3 and #4 (b). The foreseen SiC thickness to be consumed by the oxidation process is indicated in both the figures.

Table 1
Energy of ion implantation E_{impl}, dose of implantation N_{impl}, oxide thickness and thickness of consumed SiC layer during oxidation T_{ox}/T_{con}, N concentration at the oxide–SiC interface N_{inter}, total amount of N inside the oxide film N_{total}, flat-band voltage V_{fb}, effective oxide charges density N_{eff}, and interface state density D_{it} at 0.3 and 0.6 eV, for all of the samples

	E_{impl} (keV)	N_{impl} (cm^{-2})	T_{ox}/T_{con} (nm)	N_{inter} (cm^{-3})	N_{total} (cm^{-2})	V_{fb} (V)	N_{eff} (cm^{-2})	D_{it} at 0.3 eV/0.6 eV (eV^{-1} cm^{-2})
#1	–	–	60/28	1×10^{16} [a]	2.9×10^{10} [a]	+1.27	-2.6×10^{11}	$2.6 \times 10^{12}/1.8 \times 10^{11}$
#2	10	1.5×10^{13}	58/27	5×10^{18} [b]	1.2×10^{13} [b]	+0.45	$<10^{10}$	$4 \times 10^{11}/2.7 \times 10^{11}$
#3	2.5	1.0×10^{15}	53/25	1×10^{16} [a]	1.0×10^{15} [c]	+1.38	-3.5×10^{11}	$2.2 \times 10^{12}/2.2 \times 10^{11}$
#4	2.5	5.0×10^{14}	58/27	1.5×10^{19} [c]	9.9×10^{14} [c]	+0.55	$<10^{10}$	$4 \times 10^{11}/1.7 \times 10^{11}$
	5.0	5.0×10^{14}						

[a] Epilayer doping.
[b] From SRIM simulations.
[c] From SIMS analyses.

allow us to investigate the following different conditions: (i) low N concentration both in the oxide and at the interface (sample #1), (ii) low amount of N in the oxide and high N concentration at the interface (sample #2), (iii) high amount of N in the oxide and low N concentration at the interface (sample #3), and (iv) high amount of N in the oxide and high N concentration at the interface (sample #4).

Rutherford backscattering spectrometry in chanelling (RBS-C) configuration was used to measure the number of displaced atoms in each implanted sample. 1.5 MeV He^+ beam, 170° backscattering angle, and $\langle 0001 \rangle$ alignment were used. The energy resolution of the measured spectra is 15 keV. The RBS-C analysis of samples #2, #3 and #4 is reported in Fig. 2. For comparison, random and $\langle 0001 \rangle$ axis spectra of virgin 4H–SiC are also shown in the figure. The ion damage layers are at the sample surface and their thicknesses are thinner than the depth resolution of the RBS-C analysis. This means that the damage profiles cannot be resolved in depth, but the integral of the displaced Si plus C atoms can be accurately computed (±3%) by using the RUMP code [17]. The integral of Si plus C displaced atoms is 5×10^{15} cm^{-2}, 1.3×10^{16} cm^{-2}, 1.0×10^{17} cm^{-2} and 1.3×10^{17} cm^{-2} for the virgin, # 2, #3 and #4 samples, respectively. Within the hypothesis that the profiles of the displaced atoms and the ones of the N implanted atoms (see Fig. 1) are similar, and taking into account that the atomic density of SiC is 9.64×10^{22} cm^{-3}, we can affirm that in samples #3 and #4 amorphous layers of thickness 9.6 and 11.4 nm, respectively, are present at the sample surface. On the contrary, in sample #2 the implant damage is very weak; in fact, its spectrum is very closed to the one of the virgin 4H–SiC. As sample #1 was not implanted it can be assumed equal to the virgin sample.

All the samples were thermally oxidized in a wet ambient. Aiming to consume a SiC layers of ~27 nm for all of them, we carried out the wet oxidations of samples #1 and #2 at the temperature of 1100 °C for 8 h, and that of samples #3 and #4 in two steps: first at 850 °C for 30 min and then at 1100 °C for 6 h [18]. For samples #1 and #2 the process conditions have been fixed considering the oxidation kinetics of the crystalline silicon-face SiC [19]. For samples #3 and #4, which present a surface amorphous layer, a low temperature oxidation process was firstly performed to produce a fast oxidation of the amorphous layer before any recrystallisation [18]. The subsequent high temperature process was carried out in order to consume the desired thickness of about 27 nm of SiC. We underline the dramatic difference in the oxidation rate between amorphous and crystalline SiC. In the first case the oxide growth occurs with 2.5 nm/min at 850 °C [18], while in the latter case the oxidation rate at 1100 °C reduces of more than one order of magnitude [19].

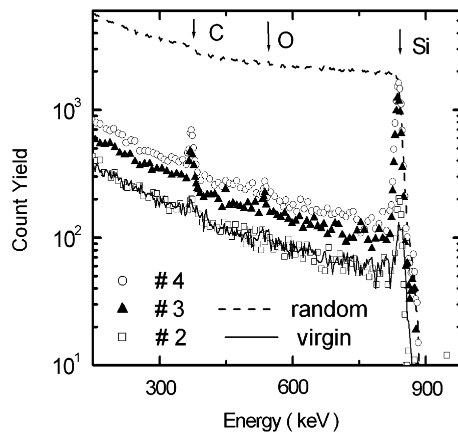

Fig. 2. $\langle 0001 \rangle$ axis RBS-C spectra of the as-implanted samples #2, #3 and #4. The random and $\langle 0001 \rangle$ axis spectra of a virgin 4H–SiC crystal are also shown for comparison. The surface energy edges of C, O and Si elements are shown by arrows.

MOS capacitors were fabricated by using aluminum for the gate oxide-electrodes and nickel for the ohmic contact on the back of the specimens. The diameter of aluminum dots deposited for gate electrodes was 800 μm and the metal overlaps 25 μm on the field oxide. Post metallization anneal was performed in forming gas at 400 °C for 30 min.

Capacitance–voltage (*C–V*) measurements were performed with a Keithley K82 system. High-frequency (HF) and quasi-static (QS) *C–V* characteristics at room temperature were measured simultaneously to avoid misalignment of the two *C–V* curves due to charge state changes and displacement of mobile ions in the oxide, typical of sequentially mode. The HF measurements were carried out at 100 kHz [20–22] with a small signal amplitude of 15 mV. In order to verify that the interface states do not follow the HF signal at 100 kHz, CV measurements were performed at 40 kHz on few samples obtaining similar results. The QS characteristics were measured with delay times of 0.1 and 2 s using a voltage step of 20 mV. We swept the gate-voltage from accumulation to depletion (AD) and from depletion to accumulation (DA). The interface state density was estimated by using the High-low method [23]. It is well known that the time constant for the emission of the trapped electrons to conduction band is [23]:

$$\tau_n = \frac{1}{\sigma_n v_{\text{th}} N_{\text{C}}} \exp\left(\frac{E_{\text{C}} - E_{\text{T}}}{kT}\right) \quad (1)$$

where σ_n (of the order of 10^{-12} cm^{-2}) is the electron capture cross section, v_{th} ($8.7 \times 10^5 \times T^{1/2}$ m/s) is the average thermal velocity of electrons, N_{C} ($3.25 \times 10^{15} \times T^{3/2}$ cm^{-3}) is the density of states in the conduction band for the 4H–SiC polytype, E_{T} is the interface trap energy in the SiC bandgap and T (K) is the temperature. Considering Eq. (1) at room temperature and our High-low *CV* measurement conditions (HF at 100 kHz and QS with delay time of 2 s), the interface traps related to E_{T} in the range 0.3–0.6 eV from the conduction band can be accurately measured.

3. Results

Fig. 3a compares the HF *C–V* curves for sample #2 sweeping the gate-voltage from accumulation to depletion and reverse from depletion to accumulation. The measurements do not evidence any large hysteresis, indicating the density of slow traps should be low. Fig. 3b shows the QS *C–V* curves collected with different delay times sweeping the gate-voltage from accumulation to depletion. These delay times differ of a factor 20. The near coincidence of the two curves reveals that the shorter delay time of 0.1 s is long enough to collect all of the interface states. This result confirms that the density of the slow traps is very low. The above reported features have been reproducible for all the samples.

Fig. 4 shows HF *C–V* curves for all of the samples in case of sweeping from accumulation to depletion. From the capacitance data of Fig. 4 we evaluated the values of oxide thickness (T_{ox}), flat-band voltage (V_{fb}) and effective oxide charges density normalized by elementary charge (N_{eff}), which are listed in Table 1. It is well known that the N_{eff} values measured in this way include the oxide trapped charges, fixed oxide charge, mobile charges and the interface charges trapped by slow traps [24]. From the experimental value of T_{ox} extracted from *CV* measurements we estimated the thickness of the SiC layer consumed during oxidation (T_{con}), and these values are also reported in Table 1. The value of 0.47 [25] was used as the thickness ratio of the consumed SiC to the grown SiO_2. As scheduled in our experiment the T_{con} value is roughly the same in each family of the MOS device. The N concentration at the oxide–SiC interface (N_{inter}) and the total number of N atoms inside the SiC layer consumed during oxidation (N_{total}) were estimated on the basis of the T_{con} values and of the profiles of Fig. 1a and b. For this determination we consider the N inside the SiC immobile during the post-implantation thermal oxidation process [26] and we neglect any N segregation effect at the SiO_2/Si interface. Furthermore, when available, the SIMS datum was preferred to the simulated one for the computation of N_{inter} and N_{total}. The obtained data are reported in Table 1. Looking at the couple of N_{inter} and N_{total} values reported for each specimen in Table 1, we can see that samples #1–#4 actually satisfy the desired conditions (i)–(iv).

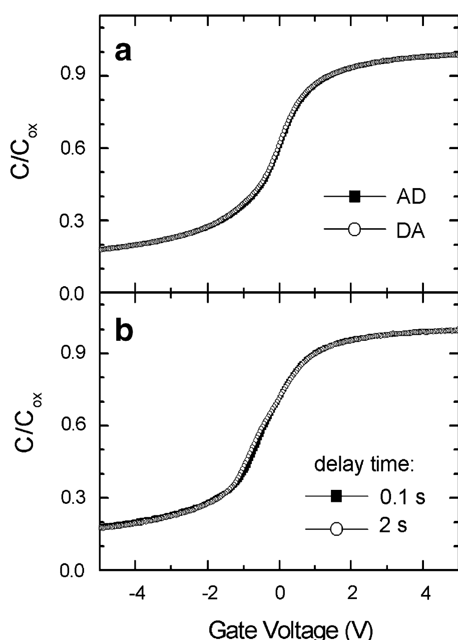

Fig. 3. HF *C–V* curves in the cases of sweeping from accumulation to depletion (AD) and from depletion to accumulation (DA) (a), and QS *C–V* curves for different delay times in case of AD (b). The *C–V* curves refer to sample #2 (N implanted at low dose), but similar behavior was observed for all the samples.

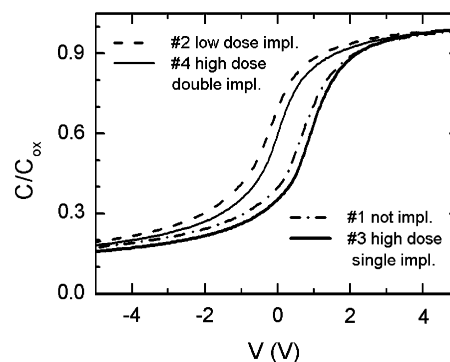

Fig. 4. Comparison among the HF *C–V* curves of all the samples processed for this study. These *C–V* curves were measured sweeping from accumulation to depletion.

Measurements of the carrier concentration in the epilayer below the oxide obtained by *C–V* curves did not evidence any variation of the donor concentration in the SiC substrate. However, the *C–V* measurements are not able to explore the effective doping concentration in the region next the SiO_2/SiC interface (about 35 nm in depth for our samples).

MOS devices of sample #1 and #3 have similar V_{fb} value ($\sim$1.3 V), the same occurs for MOS devices of specimens #2 and #4 ($\sim$0.5 V). N_{eff} reveals the presence of effective negative charges in amount of 3×10^{11} cm^{-2} for samples #1 (not implanted) and #3 (high dose single implantation), and lower than 10^{10} cm^{-2} (minimum resolution of our measurements) for samples #2 (low dose implantation) and #4 (high dose double implantation).

By using the High-low method the energy distributions of interface states density were calculated. As an example, the comparisons between the HF and QS *C–V* curves for sample #1 (not implanted) and sample #4 (high dose double implantation) are plotted in Fig. 5. The lower difference between HF and QS *C–V* curves observed for the sample #4 denotes a better electrical quality of the interface associated to this oxidation procedure. The D_{it} distributions in the energy range between 0.3 and 0.6 eV from the conduction band are shown in Fig. 6 for all the samples. Two trends of D_{it} curves can be recognized: the first one is given by the D_{it} distributions of samples #1 and #3, and the sec-

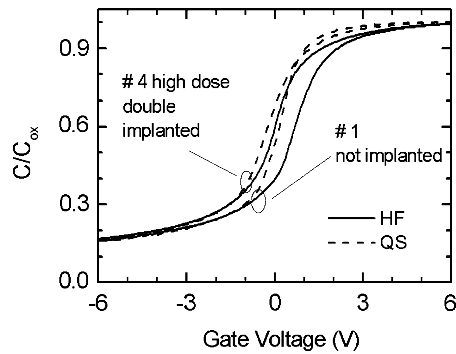

Fig. 5. Comparison between HF and QS *C–V* curves for sample not implanted (#1) and high dose double implanted (#4). All of the *C–V* curves are obtained sweeping from accumulation to depletion and for QS *C–V* curves with a delay time of 2 s.

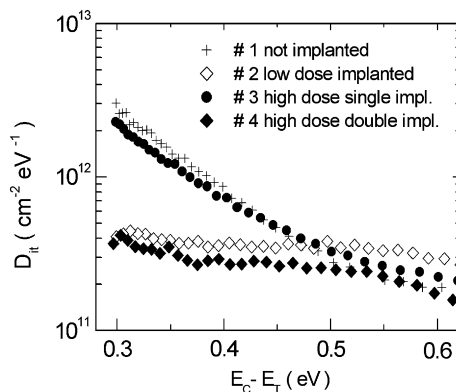

Fig. 6. Energy distributions of the interface state density D_{it} for all the samples. The data were computed by using the HF and QS measurements done sweeping from depletion to accumulation and for QS *C–V* curves with a delay time of 2 s.

ond one by those of samples #2 and #4. Specimens #1 and #3 have a decreasing D_{it} from $3\times10^{12}\,cm^{-2}$ at 0.3 eV towards $1\times10^{11}\,cm^{-2}$ at 0.6 eV. While specimens #2 and #4 have an almost constant D_{it} distribution, in fact, it goes from $3\times10^{11}\,cm^{-2}$ at 0.3 eV to $1–2\times10^{11}\,cm^{-2}$ at 0.6 eV. The D_{it} values at the edges of the range 0.3–0.6 eV are reported in Table 1 for each sample.

4. Discussion

The results of our study summarized in Table 1, evidence that two of the oxidation procedures here investigated are effective to reduce the density of states at the SiO_2/SiC interface. Both these processes (samples #2 and #4) give rise to a high N concentration at the interface ($\geqslant 5\times10^{18}\,cm^{-3}$), thus indicating a determinant role of the N in the reduction of the D_{it} in the energy range near the conduction band. Furthermore, both these processes results in N_{eff} values down to the minimum value detectable by the *C–V* method ($\sim10^{10}\,cm^{-2}$), in spite of the strong difference of the N implanted dose and of the total amount of N in the oxide ($N_{tot} = 1.2\times10^{13}\,cm^{-2}$ in #2 and $9.9\times10^{14}\,cm^{-2}$ in #4). Moreover, the presence of a high concentration of N into the oxide, with low concentration at the interface does not produce any significant change in the properties of the MOS device (see Table 1, sample #3 compared with sample #1). Differently to the conclusions reported by Ciobanu et al. [10–12], we do not observe any correlation between the shift of the V_{fb} towards negative values and the N implantation dose (see Table 1), even if in this study the N doses are much higher than those used in Ref. [12]. Looking at the data in Table 1, the V_{fb} value obtained in our study seems more linked to the value of the N concentration at the SiO_2/SiC interface than to the N integrated within the oxide. Therefore, our results do not evidence the generation of fixed positive charge into the oxide as a consequence of a high dose N implantation. The only effect of the N implantation consists in reducing the interface state density when it is located in high concentrations at the oxide–SiC interface. The decrease of D_{it} shifts the V_{fb} towards negative values and therefore the calculated N_{eff} value results strongly reduced for both the sample #2 and #4, showing an independence of N_{eff} on the used N fluence. These results indicate that a N implantation process done before a wet oxidation is effective in reducing the SiO_2/SiC interface state density near the conduction band only if an high N concentrations remains at the oxide–SiC interface.

The comparison between the samples #2 and #4 (see Table 1) shows that the employment of high N fluences with the aim to make amorphous a surface SiC layer, and thus increase the oxidation rate, can be exploited. In fact, the D_{it} and V_{fb} values of these two samples are very similar. Both the samples were implanted but specimen #2 was almost crystalline while specimen #4 had an amorphous surface layer. Both the samples have similar N concentration value at the SiO_2/SiC interface. Such N concentration is two orders of magnitude higher than the net donor concentration in the n-type epilayer 4H–SiC film and it should correspond to the presence of an ion damage even if weak. Previous investigations [27] show that at 1100 °C a SiC ion damaged crystal partially recovers, but extended defects can form. However, both these phenomena, i.e. the presence of implanted N atoms and residual damage in proximity of the surface do not degrade the electrical characteristics of the MOS devices. In particular, the formation of an amorphous SiC layer allows a faster oxidation process [14] without inducing negative effects on the SiO_2/SiC interface.

5. Conclusions

Characterization of MOS capacitors fabricated on 4H–SiC pre-implanted with N was performed and the results are presented. The proposed process, in which N is ion-implanted on SiC layer before a wet oxidation, is effective to reduce the density of interface states near the conduction band edge if an high concentration of N is introduced at the SiO_2/SiC interface. We found that only the N present

at the oxide–SiC interface improves the quality of this interface. Moreover, we do not observe any detrimental effect due to the presence of a high amount of implanted N inside the oxide. Furthermore, the possibility to obtain a faster oxidation rate by processing a N preamorphized SiC layer is confirmed.

Our results demonstrate that by using a suitable N ion implantation and an appropriate wet oxidation treatment, it is possible to obtain a reduced thermal budget process able to decrease the D_{it} near the conduction band edge. The proposed approach should be interesting for the development of the MOSFET technology on SiC in order to improve the channel mobility.

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References

[1] C. Raynaud, J. Non Cryst. Solid 1 (2001) 280.
[2] V.V. Afanas'ev, A. Stesmans, Appl. Phys. Lett. 71 (1997) 3844.
[3] R. Singh, Microelectron. Reliab. 46 (2006) 713.
[4] L.A. Lipkin, J.W. Palmour, J. Electron. Mater 25 (1996) 909.
[5] K. Fukuda, W.J. Cho, K. Arai, S. Suzuki, J. Senzaki, T. Tanaka, Appl. Phys. Lett. 77 (2000) 866.
[6] A. Poggi, F. Moscatelli, A. Scorzoni, G. Marino, R. Nipoti, M. Sanmartin, Mater. Sci. Forum 527–529 (2006) 979.
[7] S. Dimitrijev, P. Tanner, H.B. Harrison, Microelectron. Reliab. 39 (1999) 441.
[8] J.R. Williams, G.Y. Chung, C.C. Tin, K. McDonald, D. Farmer, R.K. Chanana, R.A. Weller, S.T. Pantelides, O.W. Holland, M.S. Das, L.C. Feldmann, Mater. Sci. Forum 389S–393S (2002) 96.
[9] V.V. Afanas'ev, A. Stesmans, F. Ciobanu, G. Pensl, K.Y. Cheong, S. Dimitriev, Appl. Phys. Lett. 82 (2003) 568.
[10] F. Ciobanu, G. Pensl, V.V. Afanas'ev, A. Schoner, Mater. Sci. Forum 483–485 (2005) 693.
[11] G. Pensl, F. Ciobanu, T. Frank, D. Kirfmse, M. Krieger, S. Reshanov, F. Schmid, M. Weidner, T. Oshima, H. Itoh, W.J. Choyke, Microelectron. Eng. 83 (2006) 146.
[12] F. Ciobanu, T. Frank, G. Pensl, V.V. Afanas'ev, S. Shamuilia, A. Schoner, T. Kimoto, Mater. Sci. Forum 527–529 (2006) 991.
[13] A. Poggi, R. Nipoti, S. Solmi, L. Vanzetti, Mater. Sci. Forum 457–460 (2004) 1357.
[14] A. Poggi, R. Nipoti, S. Solmi, M. Barozzi, L. Vanzetti, J. Appl. Phys. 95 (2004) 6119.
[15] A. Poggi, A. Parisini, R. Nipoti, S. Solmi, Appl. Phys. Lett. 86 (2005) 121907.
[16] SRIM2003 (<http://www.srim.org>).
[17] L.R. Doolittle, Nucl. Instrum. Meth. B 9 (1985) 344.
[18] R. Nipoti, A. Parisini, A. Poggi, Mater Sci. Forum 389–393 (2002) 1109.
[19] M.R. Melloch, J.A. Cooper, MRS Bull. 22 (1997) 42.
[20] W. Cho, R. Kosugi, J. Senzaki, K. Fukuda, K. Arai, S. Suzuki, Appl. Phys. Lett. 77 (2000) 2054.
[21] K.Y. Cheong, W. Bahng, N.K. Kim, Microelectron. Eng. 83 (2006) 65.
[22] G. Pensl, F. Ciobanu, T. Frank, D. Kirmse, M. Krieger, S. Reshanov, F. Schmid, M. Weidner, T. Ohshima, H. Itoh, W.J. Choyke, Microelectron. Eng. 83 (2006) 146.
[23] J.A. Cooper, Phys. Status Solid A 162 (1997) 305.
[24] J. Campi, Y. Shi, Y. Lou, F. Yan, J.H. Zhou, IEEE Trans. Electron. Dev. 46 (1999) 511.
[25] The ratio of T_{ox}/T_{con} was computed as the ratio (mole number of SiO_2 per unit volume)/(mole number of SiC per unit volume), resulting in ~0.47. Where, we used the values of 2.2 and 3.2 g/cm^3 for densities of SiO_2 and SiC, respectively, and those of 60.1 and 40.1 g/mol as weights per mole of SiO_2 and SiC, respectively.
[26] G.J. Phelps, N.G. Wright, E.G. Chester, C.M. Jonson, A.G. O'Neill, S. Ortolland, A. Horsfall, K. Vassilevski, R.M. Gwilliam, P.G. Coleman, C.P. Burrows, Appl. Phys. Lett. 80 (2002) 228.
[27] R. Nipoti, A. Parisini, Phys. Mag. B 80 (2000) 647.