

## Characterization of MOS capacitors fabricated on n-type 4H-SiC implanted with nitrogen at high dose

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**Abstract.** Aiming to minimize the interface state density, we fabricated MOS capacitors on n-type 4H-SiC by using wet oxidation of nitrogen implanted layers. We investigated a wide range of implantation dose, including a high dose able to amorphise a surface SiC layer with the intent to reduce the oxidation time. The oxide quality and the SiO<sub>2</sub>-SiC interface properties were characterized by capacitance-voltage measurements of the MOS capacitors. The proposed process, in which nitrogen is ion-implanted on SiC layer before a wet oxidation, is effective to reduce the density of interface states near the conduction band edge if a high concentration of nitrogen is introduced at the SiO<sub>2</sub>-SiC interface. We found that only the nitrogen implanted at the oxide-SiC interface reduces the interface states and we did not observe the generation of fixed positive charges in the oxide as a consequence of nitrogen implantation. Furthermore, the concentration of the slow traps evaluated from the Slow Trap Profiling technique was low and did not depend on the nitrogen implantation fluence.

### Introduction

Among the wide bandgap materials, silicon carbide (SiC) is an attractive material for high temperature and high power devices because of its remarkable thermal and electronic properties [1]. SiC has the added advantage of a thermally grown native oxide, which opens the opportunity for its use in metal-oxide-semiconductor (MOS) devices. Although many groups have attempted to develop SiC power MOS field-effect transistor (MOSFET), there is the great obstacle of the extremely low channel mobility, which is a main cause of a large on-resistance [2]. Interface traps generated during thermal oxidation are recognized as the major reasons for the insufficient 4H-SiC MOSFET performance. Nitridation processes using NO or N<sub>2</sub>O gas are regarded as a promising method to improve the SiO<sub>2</sub>-SiC interface characteristics [3]. Recently, nitrogen (N) implantation has been used as pre-oxidation process for the fabrication of 4H-SiC MOS capacitors obtaining a significant reduction of the interface state density in the case of the n-type material, but not in the case of the p-type one. However, the reported results obtained with dry oxides show a drawback of the N implantation process: the density of the fixed positive charges proportionally increases with the implanted nitrogen dose [4,5], giving rise to an unwanted shift of the flat-band voltage.

In this work, with the purpose to reduce the interface state density, we fabricated MOS capacitors by using wet oxidation of N<sup>+</sup> implanted SiC layers. We investigated a wide range of implantation dose, including a high dose able to amorphize a surface SiC layer with the aim to reduce the oxidation time [6]. The oxide quality and the SiO<sub>2</sub>-SiC interface properties were characterized by capacitance-voltage (C-V) measurements of the MOS capacitors. Furthermore, we employed the Slow Trap Profiling (STP) technique to estimate the number of the slow traps.

## Experimental

MOS capacitors were fabricated on a homo-epilayer grown on 8° off-axis, Si face, n-type, 4H-SiC wafer. The n-type epi-layer was 6 μm thick and had a nominal N doping density of  $1 \times 10^{16} \text{ cm}^{-3}$ . The wafer was cut in quarters in order to obtain four samples (#1- #4). A field oxide (0.6 μm) was deposited by CVD technique and patterned to open circular gate geometry of 750 μm in diameter. The samples were treated to investigate the following different conditions: i) low N concentration both in the oxide and at the interface (sample #1), ii) low amount of N in the oxide and high ( $\geq 10^{17} \text{ cm}^{-3}$ ) N concentration at the interface (sample #2), iii) high ( $10^{15} \text{ cm}^{-2}$ ) amount of N in the oxide and low N concentration at the interface (sample #3), and iv) high amount of N both in the oxide and at the interface (sample #4). Room temperature implantation was performed to introduce the nitrogen. Pearson IV simulations of the as-implanted N profiles were used to adjust the implantation and the oxidation processes. Considering the N distributions shown in Fig. 1, the consumption of ~ 27 nm of SiC during the oxidation would allow us to obtain the samples #2- #4 according with the requirements ii)-iv) above reported. Table 1 presents the implantation and oxidation conditions used for each samples. The MOS structures of sample #1 were obtained without any N implantation process and performing a standard wet oxidation at 1100 °C [7]. Samples #3 and #4 were N implanted with single and double energy, respectively, in order to obtain an amorphous layer just below the sample surface in both the samples, but different N concentrations at the SiO<sub>2</sub>-SiC interface. On these samples a low temperature (850 °C) wet oxidation process was firstly performed to have the fast oxidation of the amorphous layer without any recrystallization [6]. Sample #2 was implanted with N at a lower dose and higher energy to avoid the SiC amorphization and accumulate N around SiO<sub>2</sub>-SiC interface, then was oxidized in the same condition of sample #1. SIMS profiles (not here reported) confirmed the achievement of the demanded N distribution in the implanted samples. Sputtered aluminium has been used to fabricate the metal gates, whereas nickel has been deposited for the back contact. Post metallization anneal has been performed in forming gas at 400 °C for 30 min.

The oxide quality and the SiO<sub>2</sub>-SiC interface properties have been characterized by C-V measurements of the MOS capacitors. Simultaneous high frequency (HF) and quasi-static (QS) C-V characteristics have been obtained with a Keithley K82 System using a voltage step of 20 mV. The HF characteristics have been performed at 100 kHz, and the QS characteristics have been executed with a delay of 2 s. All the C-V measurements have been done at room temperature in the dark. Interface trap density ( $D_{it}$ ) has been determined by high-low C-V measurements, while to investigate border trap presence the STP technique [8] has been utilized. Slow trap profiles have been measured using an HP4145B parameter analyzer: the gate voltage was varied in 50 mV steps and the substrate current transient, after each gate voltage step, has been measured and digitized. Integrating in time (0-1 s) and in voltage (between -2 and +2 V) the acquired data, we obtain the total slow trap density ( $TD_{st}$ ) existing in the oxide.

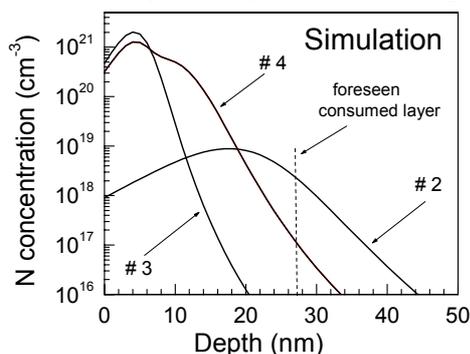


Fig.1 Pearson IV simulation of as-implanted N profiles.

	$E_{impl}$	$N_{impl}$	Low T oxidation	High T oxidation
#1	-	-	-	1100°C 8h
#2	10 keV	$1.5 \times 10^{13} \text{ cm}^{-2}$	-	1100°C 8h
#3	2.5 keV	$1.0 \times 10^{15} \text{ cm}^{-2}$	850°C 30min	1100°C 6h
#4	2.5 keV 5.0 keV	$5.0 \times 10^{14} \text{ cm}^{-2}$ $5.0 \times 10^{14} \text{ cm}^{-2}$	850°C 30min	1100°C 6h

Table 1 Energy of ion implantation  $E_{impl}$ , dose of implantation  $N_{impl}$  and oxidation for all of the samples.

## Results and discussion

MOS HF C-V measurements evaluate the gate oxide thickness of the four samples in the range 53-60 nm, therefore the thickness of the consumed SiC layer is in the range 25-28 nm. This result confirms that samples #1- #4 actually satisfy the desired condition i)-iv). Fig. 2 compares the HF C-V curves of the samples #1 and #2; for each sample the curves measured sweeping the gate-voltage from accumulation to depletion (AD) and reverse from depletion to accumulation (DA) are shown and do not evidence any large hysteresis, indicating that the density of the slow traps should be low. The value of the flat-band voltage  $V_{FB}$  is reported for both the samples on the figure. The energy distributions of the interface state density  $D_{it}$  for samples #1 and #2 are drawn in Fig. 3: the results obtained measuring three MOS capacitors in different zones of each sample are reported in order to stress the generic validity of the comparison. The implantation of N induces a shift of the  $V_{FB}$  towards negative voltage and reduces the  $D_{it}$  values in the energy range near the conduction band. Fig. 4 and 5 show the results of the same measurements performed on the samples #3 and #4. Taking into account that both the sample #3 and #4 are N implanted and the only difference is the amount of N at the interface (low for #3 and high for #4) we can deduce the importance of the N presence at the SiO<sub>2</sub>-SiC interface for the  $D_{it}$  reduction as well as the absence of any correlation between the shift of the  $V_{FB}$  towards negative voltage and the amount of N embedded in the oxide.

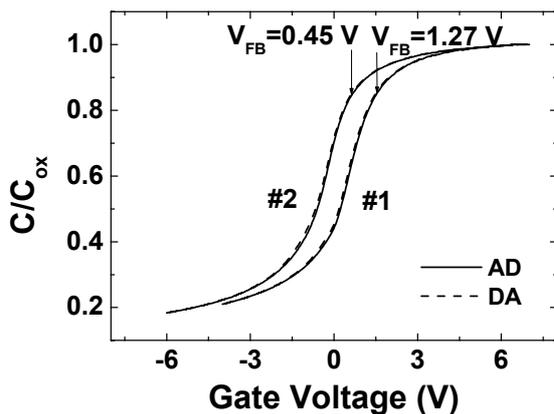


Fig. 2 Comparison between HF C-V curves measured on the samples #1 and #2.

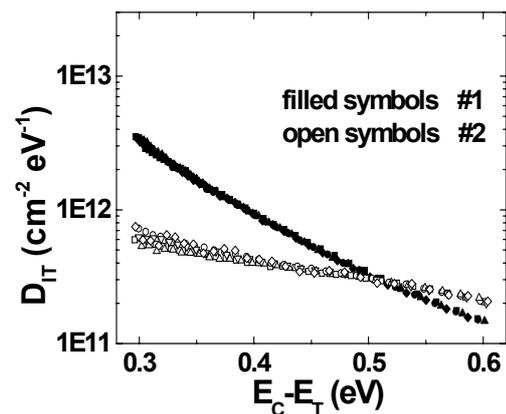


Fig.3 Energy distributions of the interface state density  $D_{it}$  obtained on the samples #1 and #2.

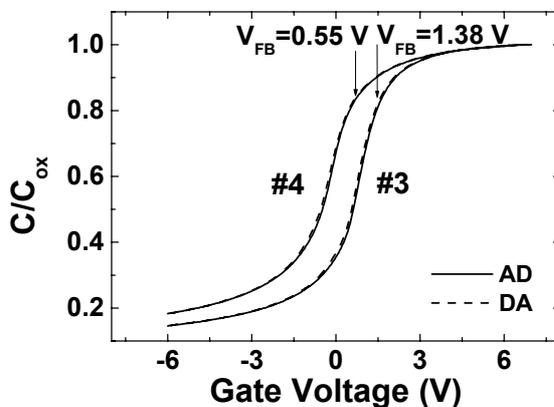


Fig. 4 Comparison between HF C-V curves measured on the samples #3 and #4.

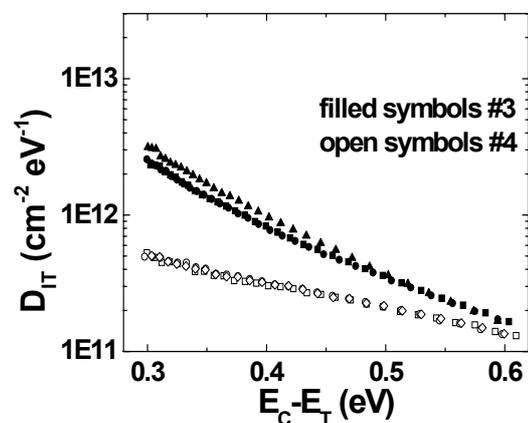


Fig. 5 Energy distributions of the interface state density  $D_{it}$  obtained on the samples #3 and #4.

	$N_{\text{inter}}$	$N_{\text{total}}$	$N_{\text{eff}}$ ( $\text{cm}^{-2}$ )	$D_{\text{it}}$ at 0.3 eV / 0.6 eV ( $\text{eV}^{-1}\text{cm}^{-2}$ )	$TD_{\text{st}}$ ( $\text{cm}^{-2}$ )
#1	low	low	$-2.6 \times 10^{11}$	$2.6 \times 10^{12} / 1.8 \times 10^{11}$	$2.7 \times 10^{10}$
#2	high	low	$< 10^{10}$	$4 \times 10^{11} / 2.7 \times 10^{11}$	$5.0 \times 10^{10}$
#3	low	high	$-3.5 \times 10^{11}$	$2.2 \times 10^{12} / 2.2 \times 10^{11}$	$3.7 \times 10^{10}$
#4	high	high	$< 10^{10}$	$4 \times 10^{11} / 1.7 \times 10^{11}$	$2.1 \times 10^{10}$

Table 2 N concentration at the oxide-SiC interface  $N_{\text{inter}}$ , total amount of N inside the oxide film  $N_{\text{total}}$ , effective oxide charges density  $N_{\text{eff}}$ , interface state density  $D_{\text{it}}$  at 0.3 and at 0.6 eV, and total density of the slow traps  $TD_{\text{st}}$  for all of the samples.

processes result in  $N_{\text{eff}}$  values down to the minimum value detectable by the C-V method ( $\sim 10^{10} \text{ cm}^{-2}$ ), in spite of the strong difference of the total amount of N in the oxide. Differently to the conclusions reported by Ciobanu et al. [4,5], we do not observe any correlation between the shift of  $V_{\text{FB}}$  towards negative values and the N implantation dose even if in this study the N doses are much higher than those used in ref. [5]. This result could be ascribed to the different oxidation ambient used in the two experiments. Furthermore, Table 2 reports the  $TD_{\text{st}}$  evaluated by the STP technique for all of the four samples: low trap density values, of the order of few units  $10^{10} \text{ cm}^{-2}$ , were calculated and the  $TD_{\text{st}}$  values did not depend on the amount of the implanted N.

## Conclusions

Characterization of MOS capacitors fabricated on n-type 4H-SiC pre-implanted with N was performed and the results are presented. The proposed process, in which N is ion-implanted on SiC layer before a wet oxidation, is effective to reduce the density of interface states near the conduction band edge if a high concentration of N is introduced at the SiO<sub>2</sub>-SiC interface. We found that only the N present at the oxide-SiC interface reduces the  $D_{\text{it}}$  density. Moreover, we do not observe any detrimental effect due to the presence of a high amount of N inside the oxide.

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The results of our study, summarized in Table 2, evidence that two of the oxidation procedures here investigated are effective to reduce the density of states at the SiO<sub>2</sub>-SiC interface. Both these processes (samples #2 and #4) give rise to a high N concentration at the interface, thus indicating a determinant role of the N in the reduction of the  $D_{\text{it}}$  in the energy range near the conduction band.

Furthermore, both these