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Improvement of radiation response of SiC MOSFETs under high temperature and humidity conditions

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The response of hexagonal (4H) silicon carbide (SiC) power metal–oxide–semiconductor field effect transistors (MOSFETs) to gamma-ray irradiation was investigated under elevated temperature and humid conditions. The shift in drain current–gate voltage (I_D–V_G) curves towards negative voltages and the leakage of I_D with a current hump due to elevated temperature irradiation were suppressed under high humidity conditions relative to dry conditions. This result can be explained in terms of the reduction in trapped oxide charge and oxide–SiC interface traps generated by irradiation due to the humid conditions. In addition, during irradiation at elevated temperature in humid conditions, electron traps at the oxide–SiC interface obviously decrease at doses above 100 kGy.

1. Introduction

Metal–oxide–semiconductor field effect transistors (MOSFETs) fabricated on silicon carbide (SiC) with a high thermal resistance and radiation hardness, are promising candidates as power electronic devices for decommissioning of TEPCO Fukushima Dai-ichi nuclear plant after the severe accident. Since the long-term operation of robots[1–3] is necessary for the decommissioning, the improvement of the radiation hardness of SiC MOSFETs is required. In addition, since such a decommissioning takes place not only in a high radiation environment but also under high temperature and humidity conditions, the radiation response under such extreme circumstances should be known.

In previous studies, the gamma-ray radiation responses of planar-type SiC MOSFETs were investigated.[4–6] SiC MOSFETs were irradiated up to the MGy regime and the effect of the gate oxide fabrication process on the radiation response was revealed. In addition, the radiation response of 4H-SiC power MOSFETs that are commercially produced were reported. The gamma ray response at room temperature (RT) or 398 K up to 1.5 Mrad (~15 kGy) exhibited a threshold voltage (V_{th}) shift to negative voltages as the dose increased.[7] In the case of irradiation at 398 K, the effect of thermal annealing of positive fixed oxide charge generated due to the irradiation was enhanced. Also, the gamma-ray response of SiC power MOSFETs under elevated temperatures up to the MGy regime were reported.[8,9] These studies revealed that the effective charges generated during irradiation were thermally annealed out by irradiation at 423 K. In contrast, for SiC MOSFETs irradiated at RT, V_{th} monotonically shifted to negative voltages with increasing dose. These reports signify that high temperature conditions improve the radiation hardness of SiC MOSFETs. Under realistic conditions such as the decommissioning of nuclear plants, the effect of the humidity on the radiation response should be also known, however, there are no reports on such effects for SiC MOSFETs.

In this report, the effect of humidity on the electrical properties of SiC MOSFETs irradiated with gamma-rays up to the MGy regime at elevated temperatures will be presented.

2. Experimental methods

The samples used in this study were vertical 4H-SiC power MOSFETs with a blocking voltage of 1200 V and a rated current of 20 A. The 45 nm thick gate oxide was fabricated using dry oxidation and subsequent N_2O treatment at the same temperature. The MOSFETs were mounted in "TO3P" packages. The package consists of an epoxy molding compound (EMC). Water vapor diffuses inside this compound even at room temperature and reaches the MOSFET chips.[10,11] SiC MOSFETs were irradiated with gamma-rays from a ^{60}Co source at a dose rate of 3.6 kGy (SiO_2)/h up to 2.6 MGy. SiC MOSFETs placed in an irradiation chamber were heated to 423 K under humid conditions obtained by replacing the air by steam (hereafter denoted as "Steam"). For comparison, SiC MOSFETs were also irradiated at 423 K in a N_2 atmosphere (hereafter denoted as "Dry"). After irradiation, the electric properties of the MOSFETs were measured at RT in the dark using a semiconductor parameter analyzer (Agilent 4156B). The measurement was carried out by sweeping the gate voltage, V_G, forward, i.e., from the off-state to the on-state. Additionally, the voltage sweep range was chosen to be as short as possible to prevent annealing of trapped charge during the measurement.[12–14] For the Steam devices, V_G was swept from the off-state voltage 2 V larger than that for Dry devices since the V_{th} reduction was suppressed compared with Dry. Such a difference in sweep conditions sometimes causes V_{th} variation.[15] However, we confirmed that sweeping from 2 V larger than the off-state V_G increased the threshold voltage by only 0.1 V and this was a small enough difference to allow us to compare threshold voltages V_{th} obtained for Steam and Dry devices.

Charge densities trapped in the oxide and at the interface between the oxide and semiconductor were calculated following the midgap-subthreshold technique.[16] Firstly the midgap current I_{mg} was calculated with the formula:

$$I_{mg} = 2^{1/2}\mu(W/L)(qN_A L_B/\beta)(n_i/N_A)^2 e^{\beta\Psi_s}(\beta\Psi_s)^{-1/2},$$

where W and L are channel width and length, respectively, and q, N_A, n_i, Ψ_s are the elementary charge, acceptor concentration in channel region, intrinsic carrier concentration at the absolute temperature (T), and band bending at the surface of SiC, respectively. The β is the reciprocal thermal energy (q/k_BT, where k_B is the Boltzmann constant) and L_B is the Debye length $[(\varepsilon_{sic}/(\beta q N_A))^{1/2}]$, where ε_{sic} is the permittivity of SiC. The mid gap current is defined as the current when the band bending at the surface, Ψ_s, corresponds to $\Psi_b = (k_BT/q)\ln(N_A/n_i)$. Most physical parameters used to calculate this were adopted from the Ref. 17. The dielectric constant ε_{sic} was taken to be 9.7, the intrinsic carrier concentration, n_i at RT was $5.44 \times 10^{-9}\,cm^{-3}$ and the measurement temperature was 298 K. Subsequently, the midgap voltage V_{mg} was obtained with the extrapolation of I_D–V_G curves to the value of I_{mg}. Using V_{mg}, the contribution to threshold voltage shift ΔV_{th} due to charge generated in the oxide and at the interface is defined as

$$\Delta V_{th} = \Delta V_{ox} + \Delta V_{int}, \quad (1)$$

where

$$\Delta V_{ox} = \Delta V_{mg}, \quad \Delta V_{int} = \Delta V_{th} - \Delta V_{mg},$$

where ΔV_{ox} and ΔV_{int} are the voltage shift due to the generation of oxide trapped charge and interface traps, respectively, ΔV_{mg} is the shift of V_{mg} by irradiation.

The areal densities of trapped holes in oxide ΔN_{ox} and interface state ΔN_{int} are defined as

$$\Delta N_{ox} = C_{ox}/q\Delta V_{ox}, \quad \Delta N_{int} = C_{ox}/q\Delta V_{int}, \quad (2)$$

where C_{ox} is the oxide capacitance. For as-fabricated and irradiated SiC MOSFETs, the I_D–V_G curves were extrapolated from $I_D = 10^{-10}$ and 10^{-7} A, respectively (to exclude the influence of the current humps).

3. Results and discussion

Figure 1(a) shows the I_D–V_G curves in the subthreshold region for SiC MOSFETs before and after irradiation at 473 K in Steam. The results obtained for V_G values between −4 and 0 V are detailed in Fig. 1(b). During measurement, a voltage of 10 V was applied to the drain. Dotted lines show I_D–V_G curves for SiC MOSFETs irradiated at a dose of 400 k and 10.4 MGy at 423 K under Dry conditions.[18] For SiC MOSFETs irradiated in Steam, the I_D–V_G curves shifted to negative voltages as the dose increased up to 20 kGy. However, a positive shift (recovery) was observed for doses above 20 kGy. A negative voltage shift of the I_D–V_G curve indicates that positive charges generated by the irradiation were trapped in the gate oxide.[8,9] The positive shift of the curves above 20 kGy is attributed to the release of the trapped charge in the oxide by thermal annealing during irradiation and/or negative charge trapped at the interface. The SiC MOSFETs irradiated in Steam show a smaller shift of the I_D–V_G curves than SiC MOSFETs irradiated under Dry conditions. This suggests that steam/water suppresses the generation of charge trapped in the oxide. In the case of Steam, the leakage current (I_D at V_G below −2 V) increased up to 10 kGy and a current hump (I_D at V_G from −3 to −1) arose for doses up to 100 kGy. However, the leakage then decreased and the current hump decreased in size above 20 kGy [Fig. 1(b)]. Compared with the I_D–V_G curves of SiC MOSFETs irradiated under Dry conditions, these humps were less significant. For I_G–V_G curves for both Steam and Dry conditions (not shown here), no humps were observed. Hence, the gate oxide did not

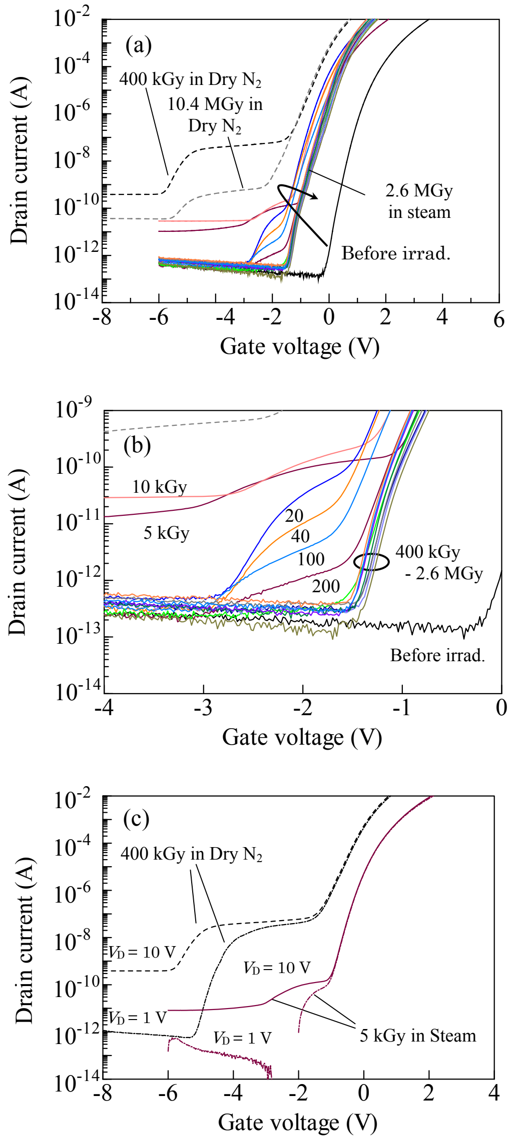

Fig. 1. (Color online) (a) I_D–V_G curves in the subthreshold region for SiC MOSFETs irradiated at 423 K under humid conditions (Steam). A V_D of 10 V was applied during the I_D–V_G measurements. For comparison, I_D–V_G curves for MOSFETs irradiated at 400 kGy or 10.4 MGy at 423 K in dry N_2 are also plotted (dotted lines). (b) The same I_D–V_G curves in the gate voltage region between −4 and 0 V. (c) I_D–V_G curves in the subthreshold region for SiC MOSFETs irradiated at 5 kGy under humid conditions and 400 kGy in dry N_2. A V_D of 1 or 10 V was applied during the I_D–V_G measurements.

serve as a leakage path.[19,20] The blocking characteristics of SiC MOSFETs irradiated under Dry conditions reported previously showed a leakage value I_D at V_D below 1200 V of around 10^{-6} A or lower even after irradiation at 10.4 MGy.[18] Also, no significant change in the breakdown voltage or leakage current was observed with increasing dose. This also suggests that the leakage path exists neither inside the gate oxide nor the p–n junction region. Figure 1(c) shows the I_D–V_G curves in the subthreshold region for SiC MOSFETs irradiated at 5 kGy in Steam and at 400 kGy under Dry conditions. During the I_D–V_G measurements, a drain voltage (V_D) of 1 or 10 V was applied. For the case of Steam, noise interrupted the I_D–V_G curve for $V_D = 1$ V at $V_G = 2$ V. For MOSFETs irradiated with $V_D = 1$ V under Dry conditions, a hump became apparent at higher gate voltages compared with $V_D = 10$ V. As V_G was increased the I_D–V_G curve met the curve for $V_D = 10$ V at around $V_G = -1$ V. Thereafter, I_D for $V_D = 1$ and 10 V increased together. These results suggest the following hump formation mechanism: when low V_D is applied, the current flows from the source to drain along the channel edges, since the barrier height is somewhat lower due to parasitic bias. As V_G increases the channel edge region is inverted and a hump in the I_D–V_G curve appears. On further increasing V_G, current mainly flows through the channel region whose area is larger than that of the edge region. I_D increases proportionally to V_G as observed for ordinary MOSFETs. When V_D is set to values as high as 10 V, the current flows more easily along the channel edge region. This gives rise to large leakage current observed for $V_D = 10$ V. Further increasing V_G, the current mainly flows along the channel. When the main current path changes from channel edge to channel region, a junction of the I_D–V_G curves for $V_D = 1$ and 10 V is formed.

The formation of current humps was previously reported for irradiated silicon MOSFETs[21,22] or CMOS technology.[23–26] Although its origin is still controversial, this effect was interpreted in terms of charges accumulated in insulators rather than the gate oxide.[22–25] For example, when n-channel commercial power Si MOSFETs were irradiated at RT, accumulated charges in the surrounding field oxide (a thicker oxide than the gate oxide) formed a parasitic bias. The results obtained in this study can be explained by such a hypothesis. Furthermore, the disappearance of the hump might be caused by annealing of those anomalous charges by steam/water. Although further studies are necessary to understand this behavior, we would like to mention here that clarifying the origin of humps seems to be beyond the scope of this report.

Figure 2 shows the ΔV_{th} of SiC MOSFETs as a function of dose. V_{th} is calculated from the intersection between the V_G-axis and a line extrapolated from the curve of the square root of I_D in the saturation region and ΔV_{th} is the difference of the non-irradiated and irradiated values. Closed and open squares are for irradiation in Steam and Dry conditions, respectively. As shown in Fig. 2, ΔV_{th} for MOSFETs irradiated in Steam reduced to −2 V up to 20 kGy, and no significant change in ΔV_{th} was observed between 20 and 800 kGy. A constant value of ΔV_{th} indicates that the accumulation of positive charge generated during irradiation was balanced by the removal of charges by annealing during irradiation. Above 800 kGy, ΔV_{th} reduced again. On the other hand, for SiC MOSFETs irradiated under Dry conditions, the magnitude of ΔV_{th} increased. This result suggests that a larger amount of accumulated positive charge is induced in the oxide for MOSFETs irradiated under Dry conditions compared with that for Steam. The ΔV_{th} for SiC MOSFETs irradiated under Dry conditions reached a minimum value at 1.2 MGy, and subsequently it slightly recovered until 2.4 MGy. According to a previous report,[8] the dose dependence of ΔV_{th} for MOSFETs irradiated under Dry conditions below 1.2 MGy was quite similar to that for MOSFETs irradiated at RT. This suggests that the generation of positive charge in the low dose range did not depend on the temperature. This implies that some kind of weak covalent bonds such as silicon-silicon atoms, hydrogen atoms (Si–H), or hydroxyl groups (Si–OH) formed during the fabrication of the gate oxide were broken by irradiation, and then those might act as a precursor site for hole traps.[27–29] An almost constant value

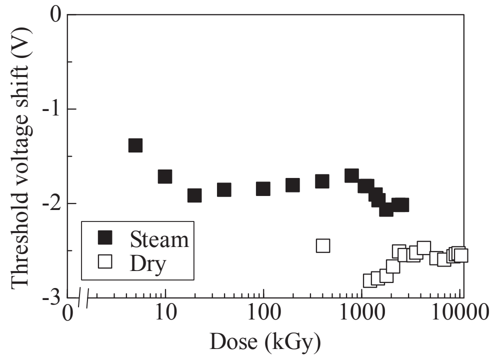

Fig. 2. Threshold voltage shift ΔV_{th} as a function of gamma-ray dose.

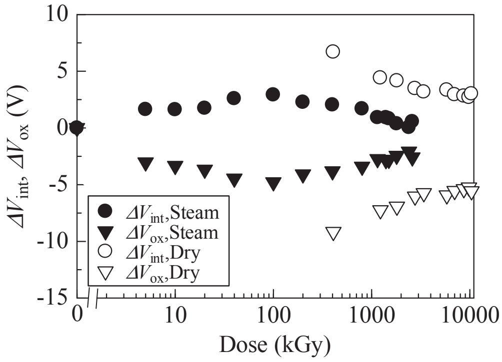

Fig. 3. Voltage shift by charge generated due to irradiation that was trapped in the oxide and at the oxide interface.

of ΔV_{th} at doses above 2.4 MGy for Dry irradiation can be interpreted in terms of competition between thermal annealing of charges and charge generation during irradiation as seen for Steam between 20 and 800 kGy. Although the detailed mechanism has not yet been clarified, we can conclude that irradiation under humid conditions is not harmful for threshold of SiC MOSFET and is in fact beneficial in harsh radiation environments.

Figure 3 shows ΔV_{ox} and ΔV_{int} for SiC MOSFETs irradiated in Steam (closed symbols) and in Dry conditions (open symbols) as a function of dose. In the case of Steam, the absolute values of both ΔV_{ox} ($|\Delta V_{ox}|$) and ΔV_{int} ($|\Delta V_{int}|$) increased with increasing dose up to 100 kGy, and the $|\Delta V_{ox}|$ was slightly larger than $|\Delta V_{int}|$. This caused the negative voltage shift of V_{th} as shown in Fig. 2. As the dose increased over 100 kGy, both $|\Delta V_{ox}|$ and $|\Delta V_{int}|$ gradually decreased. This means that in this dose region, large portion of positive charge trapped in the oxide was compensated by negative charge trapped at the interface. Above 800 kGy, the $|\Delta V_{int}|$ decreased more than $|\Delta V_{ox}|$, suggesting that positive charge trapped in the oxide is more common in this dose regime and hence the negative shift of V_{th} appeared again (see Fig. 1). On the other hand, for SiC MOSFETs irradiated under Dry conditions, a larger $|\Delta V_{ox}|$ and $|\Delta V_{int}|$ were observed in comparison with those for Steam. It should be mentioned that in dose ranges from 400 kGy to 1.8 MGy for Dry, $|\Delta V_{ox}|$ and $|\Delta V_{int}|$ might be overestimated, because the large hump was observed in I_D–V_G curves. Nevertheless, these overestimated $|\Delta V_{ox}|$ and $|\Delta V_{int}|$ values are still valid for qualitative comparison. According to the midgap-subthreshold technique, the extrapolation of I_D–V_G curves from a I_D with a value as low

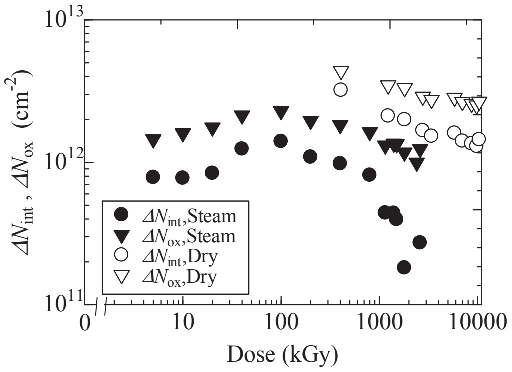

Fig. 4. Trapped charge densities as a function of irradiation dose.

as possible is recommended. Hence, we calculated $|\Delta V_{ox}|$ and $|\Delta V_{int}|$ by extrapolating of I_D–V_G curves for Steam irradiated at 1.8 MGy from lower drain current, $I_D = 10^{-12}$ A. The obtained $|\Delta V_{ox}|$ and $|\Delta V_{int}|$ are 0.2 V smaller than those in the case of extrapolation from $I_D = 10^{-7}$ A (overestimated values plotted in Fig. 3). Also, for the Dry case, the extent of the overestimation is expected to be within error. In contrast, at 1.8 MGy in Fig. 3, the difference of $|\Delta V_{ox}|$ and $|\Delta V_{int}|$ for Steam and Dry was more than 2 V. This indicates qualitatively that we can conclude that $|\Delta V_{ox}|$ and $|\Delta V_{int}|$ for the Dry case were larger than those for Steam. Above 2.8 MGy, both $|\Delta V_{ox}|$ and $|\Delta V_{int}|$ for Dry were almost constant, which signifies a balance between the accumulation and removal of charge.

In Fig. 4, the oxide (ΔN_{ox}) and interface (ΔN_{int}) trapped charge densities generated by irradiation are plotted as a function of dose. Closed and open symbols indicate SiC MOSFETs irradiated in Steam and Dry, respectively, and circles and inverse triangles denote charges trapped at the interface and those in the oxide, respectively. In the case of Steam, both ΔN_{ox} and ΔN_{int} gently increase up to 100 kGy. Above 100 kGy, they decrease with increasing dose. In the case of Dry, both ΔN_{ox} and ΔN_{int} decease with increasing dose over the dose range measured. However, both quantities are higher than those for Steam. Smaller ΔN_{ox} and ΔN_{int} for Steam compared to those for Dry indicates that steam remarkably enhances the reduction of oxide-trapped charge and interface traps during irradiation.

We now consider the possible mechanisms for the reduction of charge due to Steam. In previous reports, 4H-SiC MOS capacitors annealed in a hydrogen atmosphere at temperatures above 1073 K effectively decreased the interface trap density.[30,31] Moreover, for irradiated Si MOSFETs, a key role of hydrogen in the formation of interface traps was shown.[32] In our case, hydrogen species from the steam might be responsible for annealing the interface traps. As a result, the decrease of the interface traps gave rise to little stretch-out of subthreshold slope in I_D–V_G curves for irradiation in Steam, as shown in Fig. 1.

4. Conclusions

The radiation response of SiC MOSFETs irradiated with gamma-rays at an elevated temperature under humid conditions was investigated. Suppression of the negative shift of I_D–V_G curves and the disappearance of a leakage current hump were observed with increasing dose. When SiC MOFETs were irradiated under humid conditions at elevated temperature, a larger annealing effect of charges trapped in the oxide and at the interface was obtained in comparison with SiC MOSFETs irradiated in dry N_2. In particular, interface traps were significantly reduced above 800 kGy.

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